

# Kening Zhang

## Contact Information:

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## Education:

- Degree programs:
  - Doctor of Philosophy – Computer Engineering  
University of Central Florida – June, 2003 - present
  - Master of Science – Computer Engineering  
University of Central Florida – May 2003  
Emphasis: Computer Architecture
  - B.S of Electronic Engineering  
Xidian University - July 1998.
- Graduate Courses Taken

<u>PREFIX &amp; NUMBER</u>	<u>COURSE TITLE</u>	<u>SEM HRS</u>	<u>SEM/YR (EX. F91)</u>	<u>GRADE</u>
1.	CORE			
EEL 5708	High Performance Computer Architecture	3	F02	B
EEL 5881	Software Engineering - I	3	F02	A
EEL 5874	Expert Systems and Knowledge Engineering	3	Sp03	B+
STA 5205	Experimental Design	3	Sp04	B
CAP 5512	Evolutionary Computation	3	Sp04	B
EEL 5357	CMOS IC Design	3	F02	A
EEL 6883	Software Engineering II	3	Sp03	B
2.	OPTION			
EEL 6707	Parallel Processing	3	Sp03	A
EEL 6908	Independent Study	3	Su03	A
COT5405	Design Analysis Algorithm	3	Su03	B
EEL 5722	FPGA Design	3	F03	B
EEL 6908	Independent Study	3	F03	A
EEL 6763	Current Topics in Parallel Processing	3	F03	A
EEL 6908	Independent Study	3	Sp04	A
EEL 6908	Independent Study	3	Su04	A
EEL 5704	CAD Logical Design	3	Su04	A
EEL 7980	Dissertation	9	F04	S

### 3. Project Complete:

- Design and Modify Source Project Management System II (SPMS2) for EEL5881 Software Engineering I, Fall Semester, 2002-----Provide a Open Source project administration system based on web operation using PHP programming language,
- Polynomial Algorithm for Graph Partition for COT 5405 Design and Analysis of Algorithms, Summer Semester 2003----  
- *Two graph partitioning algorithms are presented: the canonical algorithm using dynamic programming approach with time complexity  $O(nB)$ , and an equivalent  $O(dq)$  polynomial algorithm,*
- SECDED circuit design and optimization for EEL 5722C FPGA Design, Fall Semester 2003----- An implementation of a 16-bit single error correction, double error detection (SECDED) design with a Virtex II Pro chip and optimize the power and speed performance.
- The Effective Approach to Improve Fault Tolerance in Evolvable Hardware Design for CAP5512 Evolutionary Computing, Spring Semester 2004-----*3X3 multiplier circuit under the fault tolerance in the FPGAs platforms*

### 4. Examinations

- GRE Score: 2200 (670 verbal / 770 analytical / 760 quantitative)

### 5. Publications Section

- R. F. DeMara and K. Zhang, "Autonomous FPGA Fault Handling through Competitive Runtime Reconfiguration," submitted to The NASA/DoD Conference on Evolvable Hardware (EH'05), Washington D.C., U.S.A., June 29 – July 1, 2005.

### Awards:

Special Scholarship in 1996 and 1997 in Xidian University  
Graduate Fellowship, ECE Department, University of Central Florida 2002-2003

### Professional Experience:

#### 2004 – Present: University of Central Florida – Orlando, Florida

##### Research Assistant, *Department of Electrical Engineering*

Conducting research in an Autonomous Fault Handling project funded by NASA. The project goals are to analytically model the large-scale reconfigurability of on-chip resources and to iteratively develop adaptive reconfiguration techniques to occlude failures. This novel self-regeneration approach for embedded systems is based on *Competitive Runtime Reconfiguration*. Instead of using redundant spares to handle failures, CRR synthesizes fault-specific reconfigurations to regain lost functionality. My major roles in this project include:

- *Software model of CRR,*
- *Fault tolerance model of CRR, and*
- *GA operation in CRR model.*

**2002 – 2004: University of Central Florida – Orlando, Florida**

**Teaching Assistant, Department of Electrical Engineering**

Responsible for operation of laboratories and review of technical material. Configured equipment and provided guidance to students on conducting experiments. Graded laboratories, homework, and maintained grading sheets.

- Grader for EEL 6707: Parallel Processing: 2004 Spring
- Lab for EEL 4851: Data Structure 2003 Fall, 2004 Spring, 2004 Summer
- Lab for EEL 4767: Compute System Design I 2004 Spring, 2004 Fall
- Lab for EEL 3810: Introduction to Computer Engineering 2004 Summer
- Grader for EEL 4851: Data Structure: 2003 Spring, 2003 Summer
- Grader for EEL 3210: Introduction of Engineering: 2002 Fall, 2003 Spring

**July 2001- July 2002 Beijing Advanced Digital Technology Co. Ltd**

Address: 6/F., Binhe Building D NO.1 Chedaogou, Haidian District Beijing 100089, P.R. China

R&D Software Developer of Product Development Dept.

Role: Develop format terminal interface software and financial information system for China Construction Bank Zhejiang Branch.

**July 2000 – July 2001 NetFront Inc.**

Address: Fuhua Building B2-1101 Chaoyang District Beijing 100055, P.R. China

R&D Software Developer R&D Dept.

Role: Program, test and document client side software for NetFront Security System and network security particular PKI encryption theory.

**July 1998 – July 2000 Beijing Customs**

Address: A10 Guanghua Road Chaoyang District Beijing 100026, P.R. China  
Assistant Engineer

Role: Manage and maintain electronic equipment including X-ray scanner, PCs, and peripheral devices. Provide technical support during upgrade of Beijing Customs management system.

**Technical Skills**

- *Programming Languages:* Basic, C, C++, VHDL
- *Database:* SQL server
- *Tools:* Visual Basic, Visual C++, Xilinx Explorer
- *Platform:* Unix, Linux, Windows 9x, Windows NT